|  |  |  |  |
| --- | --- | --- | --- |
|  | | **±0.1°C Accurate, 10-Bit**  **Precision Temperature Sensor** |  |
|  |
|  |  |  | |  |
|  | **Datasheet** | **RS100** | |  |
|  |  |  | |  |

**FEATURES**

**Fast Conversion Time: 5 ms**

**On-Chip Track/Hold**

**Low Total Unadjusted Error: 1 LSB**

**FUNCTIONAL BLOCK DIAGRAM**

**Full Power Signal Bandwidth: 50 kHz Single +5 V Supply**

**100 ns Data Access Time**

**Low Power (15 mW typ)**

**Low Cost**

**Standard 18-Lead DlPs or 20-Terminal Surface Mount Packages**

**GENERAL DESCRIPTION**

The RS100 is a high speed 10-bit ADC with a built-in track/ hold function. The successive approximation conversion tech-nique is used to achieve a fast conversion time of 5 s, while the built-in track/hold allows full-scale signals up to 50 kHz (386 mV/s slew rate) to be digitized. The RS100 requires only a single +5 V supply and a low cost, 1.23 V bandgap reference in order to convert an input signal range of 0 to 2 VREF.

The RS100 is designed for easy interfacing to all popular 8-bit

microprocessors using standard microprocessor control signals

(CS and RD) to control starting of the conversion and reading of

the data. The interface logic allows the RS100 to be easily

configured as a memory mapped device, and the part can be

interfaced as SLOW-MEMORY or ROM. All data outputs of

the RS100 are latched and three-state buffered to allow direct

connection to a microprocessor data bus or I/O port.

The RS100 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC2MOS) process and is available in a small, 0.3" wide, 18-lead DIP, 18-lead SOIC or in other 20-terminal surface mount packages.

REV. B

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**PRODUCT HIGHLIGHTS**

1. Fast Conversion Time/Low Power

The fast, 5 s, conversion time of the RS100 makes it suitable for digitizing wideband signals at audio and ultra-sonic frequencies while retaining the advantage of low CMOS power consumption.

1. On-Chip Track/Hold

The on-chip track/hold function is completely self-contained and requires no external hold capacitor. Signals with slew rates up to 386 mV/s (e.g., 2.46 V peak-to-peak 50 kHz sine waves) can be digitized with full accuracy.

1. Low Total Unadjusted Error

The zero, full-scale and linearity errors of the RS100 are so low that the total unadjusted error at any point on the trans-fer function is less than 1 LSB, and offset and gain adjust-ments are not required.

1. Single Supply Operation

Operation from a single +5 V supply with a low cost +1.23 V bandgap reference allows the RS100 to be used in 5 V microprocessor systems without any additional power supplies.

1. Fast Digital Interface

Fast interface timing allows the RS100 to interface easily to the fast versions of most popular microprocessors such as the Z80H, 8085A-2, 6502B, 68B09 and the DSP processor, the TMS32010.

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|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  | **(VDD = +5 V, VREF = +1.23 V, AGND = DGND = 0 V; fCLK = 4 MHz external;** | | | | |  |
| **RS100–SPECIFICATIONS all specifications TMIN to TMAX unless otherwise noted)** | | | | | | | | | | | |  |
| **Parameter** | | | | | | **J, A Versions1** | **K, B Versions** | **S Version** | **T Version** | **Units** | **Conditions/Comments** |  |
| ACCURACY | | | | | |  |  |  |  |  |  |  |
|  | Resolution | | | | | 8 | 8 | 8 | 8 | Bits |  |  |
|  | Total Unadjusted Error | | | | | ± 2 | ± 1 | ± 2 | ± 1 | LSB max |  |  |
|  | Relative Accuracy | | | | | ± 1 | ± 1/2 | ± 1 | ± 1/2 | LSB max |  |  |
|  | Minimum Resolution for Which | | | | |  |  |  |  |  |  |  |
|  | No Missing Codes Is Guaranteed | | | | | 8 | 8 | 8 | 8 | Bits max |  |  |
|  | Full-Scale Error | | | | |  |  |  |  |  |  |  |
|  | +25°C | | | | | ± 1 | ± 1 | ± 1 | ± 1 | LSB max | Full-Scale TC Is Typically 5 ppm/°C |  |
|  | TMIN to TMAX | | | | | ± 1 | ± 1 | ± 1 | ± 1 | LSB max |  |  |
|  | Offset Error2 | | | | |  |  |  |  |  |  |  |
|  | +25°C | | | | | ± 1/2 | ± 1/2 | ± 1/2 | ± 1/2 | LSB max | Offset TC Is Typically 5 ppm/°C |  |
|  | TMIN to TMAX | | | | | ± 1/2 | ± 1/2 | ± 1/2 | ± 1/2 | LSB max |  |  |
| ANALOG INPUT | | | | | |  |  |  |  |  |  |  |
|  | Voltage Range | | | | | 0 to 2 VREF | 0 to 2 VREF | 0 to 2 VREF | 0 to 2 VREF | Volts | 1 LSB = 2 VREF/256; See Figure 16 |  |
|  | DC Input Impedance | | | | | 10 | 10 | 10 | 10 | MΩ min |  |  |
|  | Slew Rate, Tracking | | | | | 0.386 | 0.386 | 0.386 | 0.386 | V/µs max |  |  |
|  | SNR3 | | | | | 45 | 45 | 45 | 45 | dB min | VIN = 2.46 V p-p @ 10 kHz; See Figure 11 |  |
| REFERENCE INPUT | | | | | |  |  |  |  |  | ± 5% |  |
|  | VREF (For Specified Performance) | | | | | 1.23 | 1.23 | 1.23 | 1.23 | Volts |  |
|  | IREF | | | | | 500 | 500 | 500 | 500 | µA max |  |  |
| LOGIC INPUTS | | | | | |  |  |  |  |  |  |  |
|  | CS | , | RD | |  |  |  |  |  |  |  |  |
|  | VINL, Input Low Voltage | | | | | 0.8 | 0.8 | 0.8 | 0.8 | V max |  |  |
|  | VINH, Input High Voltage | | | | | 2.4 | 2.4 | 2.4 | 2.4 | V min |  |  |
|  | IIN, Input Current | | | | |  |  |  |  |  |  |  |
|  | +25°C | | | | | ± 1 | ± 1 | ± 1 | ± 1 | µA max | VIN = 0 or VDD |  |
|  | TMIN to TMAX | | | | | ± 10 | ± 10 | ± 10 | ± 10 | µA max | VIN = 0 or VDD |  |
|  | CIN, Input Capacitance3 | | | | | 10 | 10 | 10 | 10 | pF max |  |  |
| CLK | | | | | |  |  |  |  |  |  |  |
|  | VlNL, Input Low Voltage | | | | | 0.8 | 0.8 | 0.8 | 0.8 | V max |  |  |
|  | VINH, Input High Voltage | | | | | 2.4 | 2.4 | 2.4 | 2.4 | V min |  |  |
|  | IINL, Input Low Current | | | | | 700 | 700 | 800 | 800 | µA max | VINL = 0 V |  |
|  | IINH, Input High Current | | | | | 700 | 700 | 800 | 800 | µA max | VINH = VDD |  |
| LOGIC OUTPUTS | | | | | |  |  |  |  |  |  |  |
|  | BUSY | | | , DB0 to DB7 | |  |  |  |  |  |  |  |
|  | VOL, Output Low Voltage | | | | | 0.4 | 0.4 | 0.4 | 0.4 | V max | ISINK = 1.6 mA |  |
|  | VOH, Output High Voltage | | | | | 4.0 | 4.0 | 4.0 | 4.0 | V min | ISOURCE = 40 µA |  |
|  | DB0 to DB7 | | | | | ± 1 | ± 1 | ± 10 | ± 10 | µA max |  |  |
|  | Floating State Leakage Current | | | | | VOUT = 0 to VDD |  |
|  | Floating State Output Capacitance3 | | | | | 10 | 10 | 10 | 10 | pF max |  |  |
| CONVERSION TIME4 | | | | | |  |  |  |  | µs |  |  |
|  | With External Clock | | | | | 5 | 5 | 5 | 5 | fCLK = 4 MHz |  |
|  | With Internal Clock, TA = +25°C | | | | | 5 | 5 | 5 | 5 | µs min | Using Recommended Clock |  |
|  |  |  |  |  |  | 15 | 15 | 15 | 15 | µs max | Components Shown in Figure 15 |  |
|  | | | | | |  |  |  |  |  |  |  |
| POWER REQUIREMENTS5 | | | | | |  |  |  |  |  | ± 5% for Specified Performance |  |
|  | VDD | | | | | +5 | +5 | +5 | +5 | Volts |  |
|  | IDD | | | | | 6 | 6 | 7 | 7 | mA max | Typically 3 mA with VDD = +5 V |  |
|  | Power Dissipation | | | | | 15 | 15 | 15 | 15 | mW typ |  |  |
|  | Power Supply Rejection | | | | | ± 1/4 | ± 1/4 | ± 1/4 | ± 1/4 | LSB max | 4.75 V ≤ VDD ≤ 5.25 V |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

NOTES

1Temperature ranges are as follows:

J, K Versions; 0ºC to +70ºC

A, B Versions; –25ºC to +85ºC

S, T Versions; –55ºC to +125ºC

2Offset error is measured with respect to an ideal first code transition that occurs at 1/2 LSB.

3Sample tested at +25ºC to ensure compliance.

4Accuracy may degrade at conversion times other than those specified.

Specifications subject to change without notice.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **RS100** | | | | |  |
|  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **TIMING SPECIFICATIONS1 (VDD = +5 V, VREF = +1.23 V, AGND = DGND = 0 V)** | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **Limit at +25**8**C** | **Limit at TMIN, TMAX** | **Limit at TMIN, TMAX** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Parameter** | | **(All Versions)** | **(J, K, A, B Versions)** | **(S, T Versions)** | **Units** |  | **Conditions/Comments** | | | | | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| t1 |  | 0 | 0 | 0 | ns min |  |  |  | to |  |  |  | Setup Time | | | | | | |  |
|  |  | CS | RD | | |  |
| t2 | 2 | 100 | 100 | 120 | ns max |  | RD | | to | | BUSY | | | | Propagation Delay | | | | |  |
| t3 | 100 | 100 | 120 | ns max | Data Access Time after | | | | | | | | | | RD |  |  | |  |
| t4 |  | 100 | 100 | 120 | ns min |  | RD | | Pulse Width | | | | | | | | | | |  |
| t5 | 2 | 0 | 0 | 0 | ns min |  | CS | to | | RD | | | Hold Time | | | | | | |  |
| t6 | 80 | 80 | 100 | ns max |  | Data Access Time after | | | | | | | | | BUSY | |  | |  |
| t7 | 3 | 10 | 10 | 10 | ns min |  | Data Hold Time | | | | | | | | | | | | |  |
|  |  | 80 | 80 | 100 | ns max |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| t8 |  | 0 | 0 | 0 | ns min |  | BUSY | | | to | | CS | | Delay | | | | |  |  |

NOTES

1Timing specifications are sample tested at +25C to ensure compliance. All input control signals are specified with tr = tf = 20 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

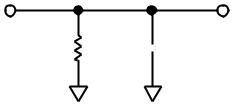
2t3 and t6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

3t7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

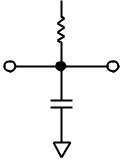
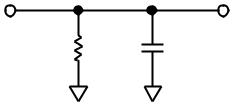
Specifications subject to change without notice.

**Test Circuits**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  | **+5V** | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  | **3k**V | | |  |
|  |  |  |  |  |  |  |  |  |  |  |
| **DBN** | |  |  |  | **DBN** |  |  |  |  |  |  |  |  |
| **3k**V |  |  |  | **100pF** |  |  |  |  |  | **100pF** | |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| **DGND** | |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | **DGND** | | |  |
|  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| *a. High-Z to VOH* | | | | | *b High-Z to VOL* | | | | | | | |  |
| *Figure 1. Load Circuits for Data Access Time Test* | | | | | | | | | | | | |  |
| **ABSOLUTE MAXIMUM RATINGS\*** | | | | |  |  |  |  |  |  |  |  |  |
| VDD to AGND . . . . . . | | | | . . . . . . . . . . . . | . . . . . . . | |  | . |  | . | –0.3 V, +7 V | |  |
| VDD to DGND . . . . . . | | | | . . . . . . . . . . . . | . . . . . . . | |  | . |  | . | –0.3 V, +7 V | |  |
| AGND to DGND . . . | | | | . . . . . . . . . . . . | . . . . . . . | |  | . |  | . | –0.3 V, VDD | |  |
| Digital Input Voltage to DGND . . . . | | | | | . . . –0.3 V, VDD + 0.3 V | | | | | | | |  |
| Digital Output Voltage to DGND . . . | | | | | . . . –0.3 V, VDD + 0.3 V | | | | | | | |  |
| CLK Input Voltage to DGND . . . . . . | | | | | . . . –0.3 V, VDD + 0.3 V | | | | | | | |  |
| VREF to AGND . . . . . | | | | . . . . . . . . . . . . | . . . . . . . | |  | . |  | . | –0.3 V, VDD | |  |
| AIN to AGND . . . . . . | | | | . . . . . . . . . . . . | . . . . . . . | |  | . |  | . | –0.3 V, VDD | |  |
| Operating Temperature Range | | | | |  |  |  |  |  | 0C to +70C | | |  |
| Commercial (J, K Versions) . . . . . . | | | | | . . . . . . . | |  | . |  |  |
| Industrial (A, B Versions) . . . . . . . | | | | | . . . . . | . –25C to +85C | | | | | | |  |
| Extended (S, T Versions) . . . . . . . . | | | | | . . . . . | –55C to +125C | | | | | | |  |



|  |  |  |  |
| --- | --- | --- | --- |
|  |  | **+5V** |  |
|  |  | **3k**V |  |
| **DBN** |  | **DBN** |  |
|  |  |  |
| **3k**V | **10pF** | **10pF** |  |
|  |  |  |
|  | **DGND** | **DGND** |  |
|  |  |  |
| *a. VOH to High-Z* | | *b. VOL to High-Z* |  |



*Figure 2. Load Circuits for Data Hold Time Test*

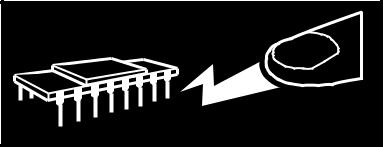
|  |  |
| --- | --- |
| Storage Temperature Range . . . . . . . . . . . . | –65C to +150C |
| Lead Temperature (Soldering, 10 sec) . . . . | . . . . . . . . +300C |
| Power Dissipation (Any Package) to +75C | . . . . . . . 450 mW |
| Derates above +75C by . . . . . . . . . . . . . . . | . . . . . . 6 mW/C |

\*Stresses above those listed under Absolute Maximum Ratings may cause perma-nent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the RS100 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**WARNING!**



**ESD SENSITIVE DEVICE**

**RS100**

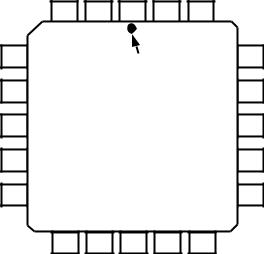
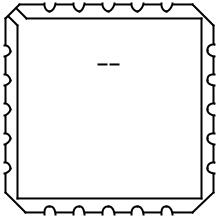
**DIP/SOIC**



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  | **VDD** |  |
| **CS** | **1** |  |  |  | **18** |  |
| **RD** |  |  |  |  |  | **VREF** |  |
| **2** |  |  |  | **17** |  |
| **TP** |  |  |  |  |  | **AIN** |  |
| **3** |  |  |  | **16** |  |
|  |  |  |  |  |  | **AGND** |  |
| **BUSY** | **4** | **RS100** | | | **15** |  |
| **CLK** |  |  | **DB0 (LSB)** |  |
| **5** | **TOP VIEW** | | | **14** |  |
| **DB7 (MSB)** |  | **(Not to Scale)** | | |  | **DB1** |  |
| **6** |  |  |  | **13** |  |
| **DB6** |  |  |  |  |  | **DB2** |  |
| **7** |  |  |  | **12** |  |
| **DB5** |  |  |  |  |  | **DB3** |  |
| **8** |  |  |  | **11** |  |
| **DGND** |  |  |  |  |  | **DB4** |  |
| **9** |  |  |  | **10** |  |
|  |  |  |  |  |  |  |  |



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **PIN CONFIGURATIONS** | | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **LCCC** | | |  |  |  |  |  |  |  | **PLCC** | | | | | | |  |  |  |  |  |
|  | **TP** | **RD** | **CS** | **DD** | **REF** |  |  |  |  | **RD** |  | **CS** | | **NC** |  |  | **DD** | | **REF** | |  |  |  |
|  | **V** | **V** |  |  |  |  |  |  |  | **V** | | **V** | |  |  |  |
|  | **3** | **2** | **1** | **20** | **19** |  |  | **3** | | | **2** | |  | **1** | **20** | | |  | **19** |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **BUSY 4** |  |  |  |  |  | **18 AIN** | **TP** | **4** |  |  |  |  |  |  | **PIN 1** | | | |  |  | **18** | **AIN** |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| **CLK 5** |  | **RS100** | | |  | **17 AGND** | **BUSY** | **5** |  |  |  |  |  |  | **IDENTIFIER** | | | | | | **17** | **AGND** |  |
|  |  |  |  |  | **RS100** | | | | | | |  |  |  |
| **DB7 (MSB) 6** |  |  | **16 DB0 (LSB)** |  |  |  |  |  |  |  |  |  |  |
|  | **TOP VIEW** | | |  | **CLK** | **6** |  |  |  |  |  | **16** | **DB0 (LSB)** |  |
|  |  |  |  |  | **TOP VIEW** | | | | | | |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| **DB6 7** | **(Not to Scale)** | | | | | **15 DB1** |  |  |  |  |  |  |  |  |  |  |
| **DB7 (MSB)** | **7** |  |  | **(Not to Scale)** | | | | | | | | | | **15** | **DB1** |  |
| **DB5 8** |  |  |  |  |  | **14 DB2** |  |  |  |
|  |  |  |  |  | **DB6** | **8** |  |  |  |  |  |  |  |  |  |  |  |  | **14** | **DB2** |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **9** | **10** | **11** | **12** | **13** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | **9** |  | **10** |  | **11** |  |  | **12** |  | **13** |  |  |  |  |
|  | **DGND** | **NC** | **NC** | **DB4** | **DB3** |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | **DB5** |  | **DGND** | | **NC** |  |  | **DB4** | | **DB3** | |  |  |  |
| **NC = NO CONNECT** | |  |  |  |  |  | **NC = NO CONNECT** | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |



**ORDERING GUIDE**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | **Relative** |  |
|  | **Temperature** | **Accuracy** | **Package** |
| **Model1** | **Range** | **(LSB)** | **Options2** |
| RS100JR | 0C to +70C | 1 max | R-18 |
| RS100JN | 0C to +70C | 1 max | N-18 |
| RS100KN | 0C to +70C | 1/2 max | N-18 |
| RS100JP | 0C to +70C | 1 max | P-20A |
| RS100KP | 0C to +70C | 1/2 max | P-20A |
| RS100AQ | –25C to +85C | 1 max | Q-18 |
| RS100BQ | –25C to +85C |  1/2 max | Q-18 |
| RS100SQ | –55C to +125C | 1 max | Q-18 |
| RS100TQ | –55C to +125C | 1/2 max | Q-18 |
| RS100SE | –55C to +125C | 1 max | E-20A |
| RS100TE | –55C to +125C | 1/2 max | E-20A |
|  |  |  |  |

NOTES

1To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87762.

2E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip, R = SOIC.

**TERMINOLOGY**

**LEAST SIGNIFICANT BIT (LSB)**

An ADC with 8-bits resolution can resolve 1 part in 28 (i.e.,

1. of full scale. For the RS100 with +2.46 V full-scale one LSB is 9.61 mV.

**TOTAL UNADJUSTED ERROR**

This is a comprehensive specification that includes full-scale error, relative accuracy and offset error.

**RELATIVE ACCURACY**

Relative Accuracy is the deviation of the ADC’s actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full-scale transition point.

**SNR**

Signal-to-Noise Ratio (SNR) is the ratio of the desired signal to the noise produced in the sampled and digitized analog signal. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantiza-tion noise. The theoretical SNR for a sine wave input is given by

*SNR* = (6.02 *N* + 1.76) *dB* where *N* is the number of bits in the ADC.

**FULL-SCALE ERROR (GAIN ERROR)**

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2 LSBs.

**ANALOG INPUT RANGE**

With VREF = +1.23 V, the maximum analog input voltage range is 0 V to +2.46 V. The output data in LSBs is related to the analog input voltage by the integer value of the following expression:

1. *AIN*

|  |  |  |  |
| --- | --- | --- | --- |
| *Data (LSBs) =* |  | *+* 0.5 |  |
| 2 *V* |  |
|  | *REF* |  |  |

**SLEW RATE**

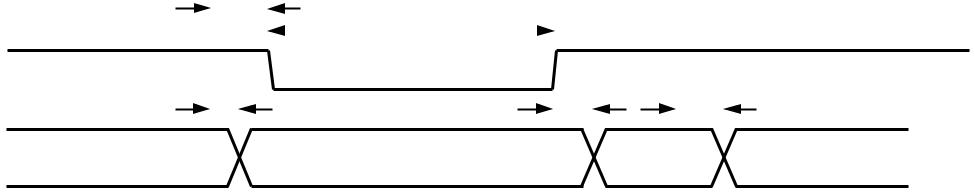
Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. Slew Rate limitations may restrict the analog signal bandwidth for full-scale analog signals below the bandwidth allowed from sampling theorem considerations.

**RS100**

**CS** 



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **t1** | | |  |  |  |  |  |  |  | **t5** | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| **RD** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **t2** | |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| **BUSY** |  |  |  | **tCONV** |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **t3** |  |  |  |  |  |  | **t6** |  |  | **t7** |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| **DATA** | **HIGH IMPEDANCE** | |  |  | **OLD DATA** | | | |  | **NEW** | |  | **HIGH IMPEDANCE** |  |
| **BUS** | |  |  |  | **DATA** | |  | **BUS** |  |
|  |  |  |  |  |  |  |  |  |  |



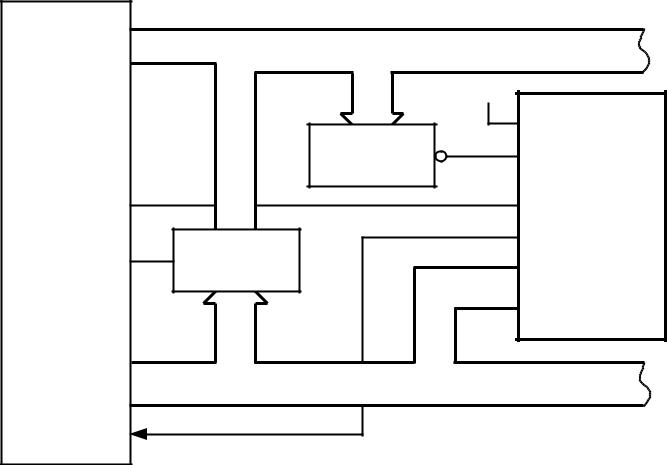
*Figure 3. Slow Memory Interface Timing Diagram*

**TIMING AND CONTROL OF THE RS100**

The two logic inputs on the RS100, CS and RD, control both the starting of conversion and the reading of data from the part. A conversion is initiated by bringing both of these control inputs LOW. Two interface options then exist for reading the output data from the RS100. These are the Slow Memory Interface and ROM Interface, their operation is outlined below. It should be noted that the TP pin of the RS100 must be hard-wired HIGH to ensure correct operation of the part. This pin is used in testing the device and should not be used as a feedthrough pin in double-sided printed circuit boards.

**SLOW MEMORY INTERFACE**

The first interface option is intended for use with microproces-sors that can be forced into a WAIT STATE for at least 5 s. The microprocessor (such as the 8085A) starts a conversion and is halted until the result of the conversion is read from the con-verter. Conversion is initiated by executing a memory READ to the RS100 address, bringing CS and RD LOW. BUSY subse-quently goes LOW (forcing the microprocessor READY input LOW), placing the processor into a WAIT state. The input signal, which had been tracked by the analog input, is held on the third falling clock edge of the input clock after CS and RD have gone LOW (see Figure 12). The RS100 then performs a conversion on this acquired input signal value. When the con-version is complete (BUSY goes HIGH), the processor com-pletes the memory READ and acquires the newly converted data. The timing diagram for this interface is shown in Figure 3.



|  |  |  |  |
| --- | --- | --- | --- |
| **A8–A15** | **ADDRESS BUS** |  |  |
|  |  | **+5V** |  |
| **8085A–2** |  | **TP** |  |
| **ADDRESS** | **CS** |  |
|  | **DECODE** |  |
|  | **RS100\*** |  |
|  |  |  |
| **S0** |  | **RD** |  |
|  | **ADDRESS** | **BUSY** |  |
| **ALE** |  |  |
| **LATCH** |  |  |
|  | **DB0–DB7** |  |
|  |  |  |
| **AD0–AD7** | **DATA BUS** |  |  |
| **READY** |  |  |  |
|  | **\*LINEAR CIRCUITRY OMITTED FOR CLARITY** | |  |
|  | **SO = 0 FOR READ CYCLES** | |  |

*Figure 4. RS100 to 8085A-2 Slow Memory Interface*

The major advantage of this interface is that it allows the micro-processor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the RS100 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, BUSY of the RS100 must go LOW very early in the cycle for the READY input to be effec-tive in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is LOW for a READ cycle) provides the READ signal to the RS100. The connection diagram for the RS100 to 8085A-2 Slow Memory interface is shown in Figure 4.

**ROM INTERFACE**

The alternative interface option on the RS100 avoids placing the microprocessor into a WAIT state. In this interface, a con-version is started with the first READ instruction, and the sec-ond READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5. It is possible to avoid starting another conversion on the second READ (see below).

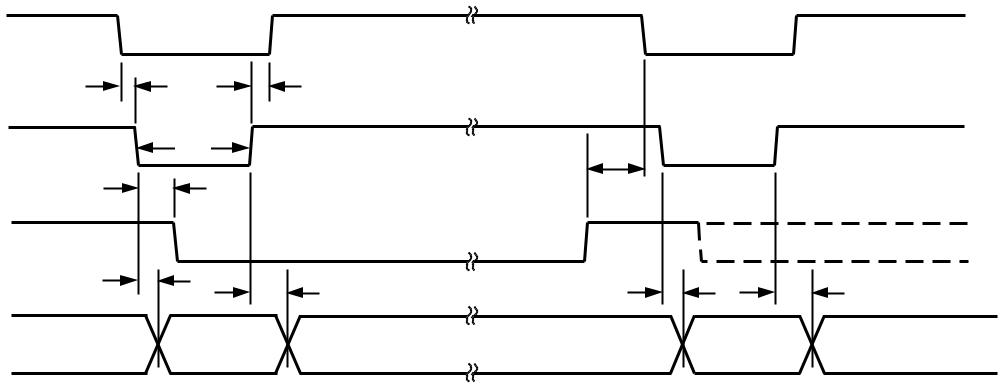
Conversion is initiated by executing a memory READ instruc-tion to the RS100 address, causing CS and RD to go LOW. Data is also obtained from the RS100 during this instruction. This is old data and may be disregarded if not required. BUSY goes LOW, indicating that conversion is in progress, and re-turns HIGH when conversion is complete. Once again, the input signal is held on the third falling edge of the input clock after CS and RD have gone LOW.

The BUSY line may be used to generate an interrupt to the microprocessor or monitored to indicate that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the RS100 conversion time. For the RS100 to operate correctly in the ROM interface mode, CS and RD should not go LOW before BUSY returns HIGH.

Normally, the second READ instruction starts another conver-sion as well as accessing the output data. However, if CS and

RD are brought LOW within one external clock period of BUSY going HIGH, a second conversion does not occur.

**RS100**



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **CS** |  |  |  |  |  |  |
|  | **t1** |  | **t5** |  |  |  |
| **RD** |  | **t4** | **t8** |  |  |  |
|  |  | **t2** |  |  |  |  |
| **BUSY** |  |  |  |  |  |  |
|  | **t3** | **t7** | **t3** |  | **t7** |  |
|  |  |  |  |
| **DATA** | **HIGH** | **OLD** | **HIGH IMPEDANCE** | **NEW** | **HIGH IMPEDANCE** |  |
| **IMPEDANCE BUS** | **DATA** | **BUS** | **DATA** | **BUS** |  |

*Figure 5. ROM Interface Timing Diagram*

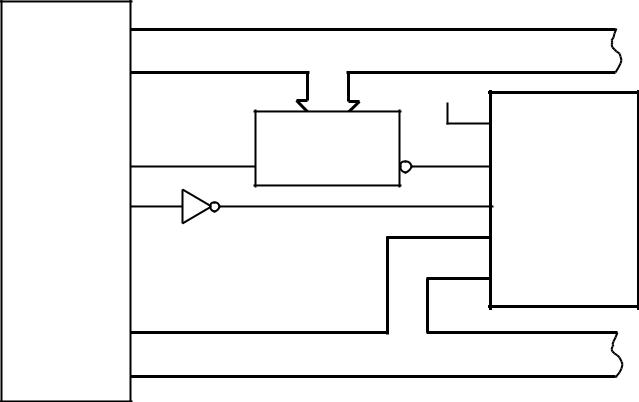
Figures 6 and 7 show connection diagrams for interfacing the RS100 in the ROM Interface mode. Figure 6 shows the RS100 interface to the 6502/6809 microprocessors while the connection diagram for interfacing to the Z-80 is shown in Figure 7.

As a result of its very fast interface timing, the RS100 can also be interfaced to the DSP processor, the TMS32010. The RS100 will (within specifications) interface to the TMS32010, running at up to 18 MHz, but will typically work over the full clock frequency range of the TMS32010. Figure 8 shows the connection diagram for this interface. The RS100 is mapped at a port address. Conversion is initiated using an IN A, PA instruction where PA is the decoded port address for the RS100. The conversion result is obtained from the part using a second IN A, PA instruction, and the resultant data is placed in the TMS32010 accumulator.

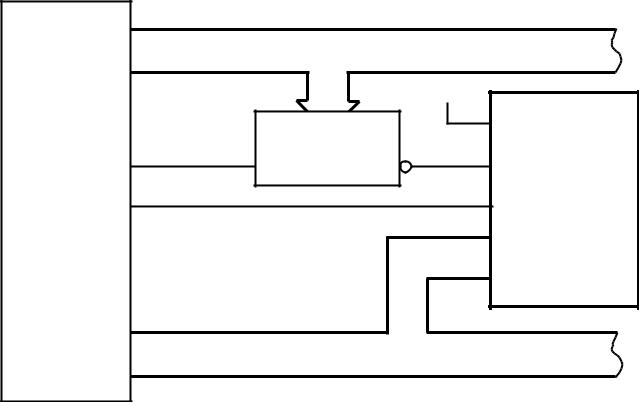
In many applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sam-pling uncertainty or jitter. The interfaces outlined previously require that for sampling at equidistant intervals, the user must count clock cycles or match software delays. This is especially difficult in interrupt-driven systems where uncertainty in inter-rupt servicing delays would require that the RS100 have prior-ity interrupt status and even then redundant software delays may be necessary to equalize loop delays.

This problem can be overcome by using a real time clock to control the starting of conversion. This can be derived from the clock source used to drive the RS100 CLK pin. Since the

|  |  |  |  |
| --- | --- | --- | --- |
| **A0–A15** | **ADDRESS BUS** |  |  |
| **6502/6809** |  | **+5V** |  |
| **ADDRESS** | **TP** |  |
|  |  |
|  |  |  |
|  | **DECODE** |  |  |
| **R/W** | **EN** | **CS RS100\*** |  |
| f**2 OR E** |  | **RD** |  |
|  |  | **DB0–DB7** |  |
| **D0–D7** | **DATA BUS** |  |  |
|  | **\*LINEAR CIRCUITRY OMITTED FOR CLARITY** | |  |



*Figure 6. RS100 to 6502/6809 ROM Interface*



**ADDRESS BUS**

**+5V**

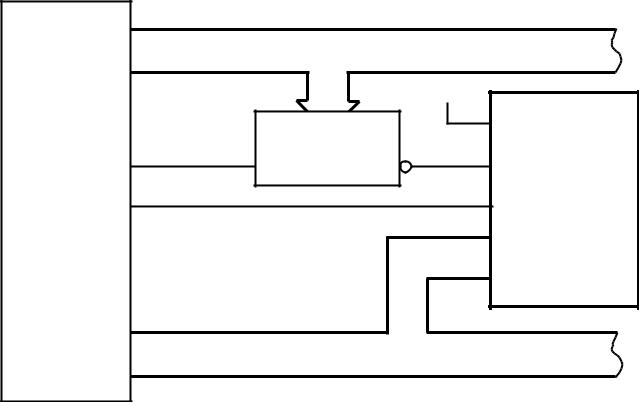
**Z–80**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | **ADDRESS** | **TP** |  |
| **MREQ** | **EN** | **DECODE** | **CS RS100\*** |  |
|  |  |
| **RD** |  |  | **RD** |  |
|  |  |  | **DB7** |  |
|  |  |  | **DB0** |  |
| **DB7** |  |  |  |  |
| **DB0** |  | **DATA BUS** |  |  |
|  |  |  |  |
|  | **\*LINEAR CIRCUITRY OMITTED FOR CLARITY** | | |  |

sampling instant occurs three clock cycles after CS and RD go LOW, the input signal sampling intervals are equidistant. The resultant data is placed in a FIFO latch that can be accessed by the microprocessor at its own rate whenever it requires the data. This ensures that data is not READ from the RS100 during a conversion. If a data READ is performed during a conversion, valid data from the previous conversion will be accessed, but the conversion in progress may be interfered with and an incorrect result is likely.

If CS and RD go LOW within 20 ns of a falling clock edge, the RS100 may or may not see that falling edge as the first of the three falling clock edges to the sampling instant. In this case, the sampling instant could vary by one clock period. If it is impor-tant to know the exact sampling instant, CS and RD should not go LOW within 20 ns of a falling clock edge.

*Figure 7. RS100 to Z-80 ROM Interface*



|  |  |  |  |
| --- | --- | --- | --- |
| **PA2** | **ADDRESS BUS** |  |  |
|  |  |  |
| **PA0** |  | **+5V** |  |
| **TMS32010** |  |  |
| **ADDRESS** | **TP** |  |
|  |  |
|  |  |  |
| **MEN** | **DECODE** |  |  |
| **EN** | **CS RS100\*** |  |
| **DEN** |  | **RD** |  |
|  |  | **DB7** |  |
|  |  | **DB0** |  |
| **D7** |  |  |  |
| **D0** | **DATA BUS** |  |  |
|  |  |  |
|  | **\*LINEAR CIRCUITRY OMITTED FOR CLARITY** | |  |

*Figure 8. RS100 to TMS32010 ROM Interface*

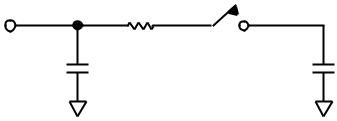
REV. B

**A SAMPLED-DATA INPUT**

The RS100 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 9. When a conversion starts, switch S1 is closed, and the equivalent input capacitance is charged to VIN. With a switch resistance of typically

500 Ω and an input capacitance of typically 2 pF, the input time constant is 1 ns. Thus CIN becomes charged to within ±1/4 LSB in 6.9 time constants or about 7 ns. Since the RS100 requires two input clock cycles (at a clock frequency of 4 MHz) before going into the compare mode, there is ample time for the input voltage to settle before the first comparator decision is made. Increasing the source resistance increases the settling time re-quired. Input bypass capacitors placed directly at the analog input act to average the input charging currents. The average current flowing through any source impedance can cause full-scale errors.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **RON** | **S1** |  |
|  | **500**V |  |
| **VIN** |  |  |
|  |  |  |
| **CS** |  | **2pF** |  |
| **0.5pF** |  |  |
|  |  |  |

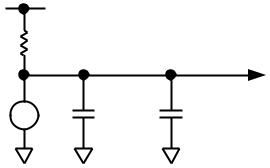


*Figure 9. Equivalent Input Circuit*

**REFERENCE INPUT**

The reference input impedance on the RS100 is code depen-dent and varies by a ratio of approximately 3-to-1 over the digi-tal code range. The typical resistance range is from 6 kΩ to 18 kΩ. As a result of the code dependent input impedance, the VREF input must be driven from a low impedance source. Figure 10 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23 V.

**+5V**



|  |  |  |  |
| --- | --- | --- | --- |
| **3.3k**V | **1.23V** |  |  |
|  |  |  |
| **+** |  |  |  |
| **AD589** | **47**m**F** | **0.1**m**F** |  |
| **–** |  |  |  |

*Figure 10. Reference Circuit*

**TRACK-AND-HOLD**

The on-chip track-and-hold on the RS100 means that input signals with slew rates up to 386 mV/µs can be converted with-out error. This corresponds to an input signal bandwidth of 50 kHz for a 2.46 V peak-to-peak sine wave. Figure 11 shows

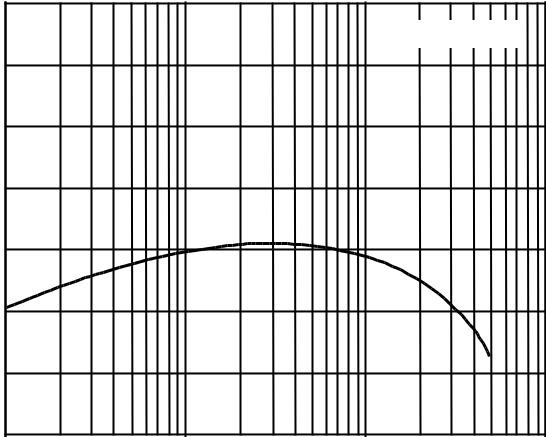
1. typical plot of signal-to-noise ratio versus input frequency over the input bandwidth of the RS100. The SNR figures are gen-erated using a 200 kHz sampling frequency, and the reconstructed sine wave passes through a filter with a cutoff frequency

of 50 kHz.

The improvement in the SNR figures seen at the higher frequen-cies is due to the sharp cutoff of the filter (50 kHz, 8th order Chebyshev) used in the test circuit.

**RS100**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **40** |  |  |  |  |
|  |  |  |  | **TA = +25**8**C** |  |
|  | **42** |  |  |  |  |
|  | **44** |  |  |  |  |
| **dB** | **46** |  |  |  |  |
| **SNR –** |  |  |  |  |
| **48** |  |  |  |  |
|  |  |  |  |  |
|  | **50** |  |  |  |  |
|  | **52** |  |  |  |  |
|  | **54** | **1k** | **10k** | **100k** |  |
|  | **100** |  |



**INPUT FREQUENCY – Hz**

*Figure 11. SNR vs. Input Frequency*

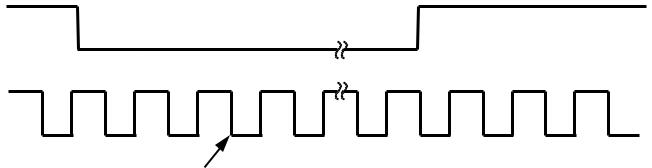
The input signal is held on the third falling edge of the input clock after CS and RD go LOW. This is indicated in Figure 12 for the Slow Memory Interface. Between conversions, the input signal is tracked by the RS100 track-and-hold. Since the sampled signal is held on a small, on-chip capacitor, it is advis-able that the data bus be kept as quiet as possible during a conversion.



**CS**



**RD**



**BUSY**

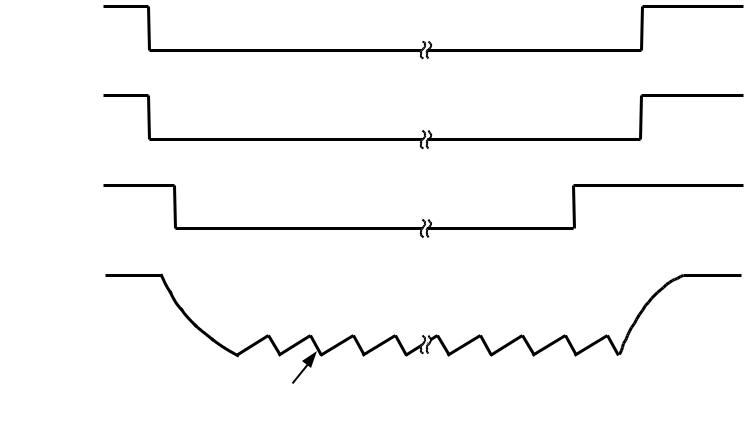
**EXTERNAL**

**CLOCK**

**INPUT SIGNAL**

**HELD HERE**

*Figure 12a. Track-and-Hold (Slow Memory Interface) with External Clock*



**CS**

**RD**

**BUSY**

**INTERNAL**

**CLOCK**

**INPUT SIGNAL**

**HELD HERE**

*Figure 12b. Track-and-Hold (Slow Memory Interface) with Internal Clock*

**RS100**

**INTERNAL/EXTERNAL CLOCK**

The RS100 can be used with its own internal clock or with an externally applied clock. In either case, the clock signal appear-ing at the CLK pin is divided internally by two to provide an internal clock signal for the RS100. A single conversion lasts for 20 input clock cycles (10 internal clock cycles).

**INTERNAL CLOCK**

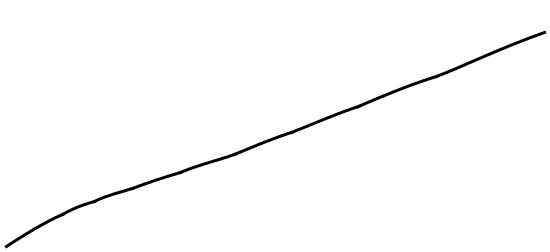
Clock pulses are generated by the action of the external capaci-

tor (CCLK) charging through an external resistor (RCLK) and discharging through an internal switch. When a conversion is

complete, the internal clock stops operating. In addition to conversion, the internal clock also controls the automatic inter-nal reset of the SAR. This reset occurs at the start of each con-version cycle during the first internal clock pulse.

Nominal conversion times versus temperature for the recom-mended RCLK and CCLK combination are shown in Figure 13.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **14** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | **RCLK =** | | **100k**V |  |  |  |  |  |  |  |  |  |  |  |  |  |
| m**–s** | **13** |  | **CCLK = 100pF** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **12** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **TIME** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **11** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **CONVERSION** | **9** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **10** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **8** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **7** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | **–25** | | **0** | | **+25** | | **+50** | | **+75** | | **+100** | | **+125** | |  |
|  | **–55** | | |  |



**AMBIENT TEMPERATURE –**8**C**

*Figure 13. Typical Conversion Times vs. Temperature Using Internal Clock*

The internal clock is useful because it provides a convenient clock source for the RS100. Due to process variations, the actual operating frequency for this RCLK/CCLK combination can vary from device to device by up to ± 50%. For this reason it is recommended that an external clock be used in the following situations:

1. Applications requiring a conversion time that is within 50% of 5 µs, the minimum conversion time for specified accuracy. A clock frequency of 4 MHz at the CLK pin gives a conversion time of 5 µs.
2. Applications where time related software constraints cannot accommodate time differences that may occur due to unit to

unit clock frequency variations or temperature.

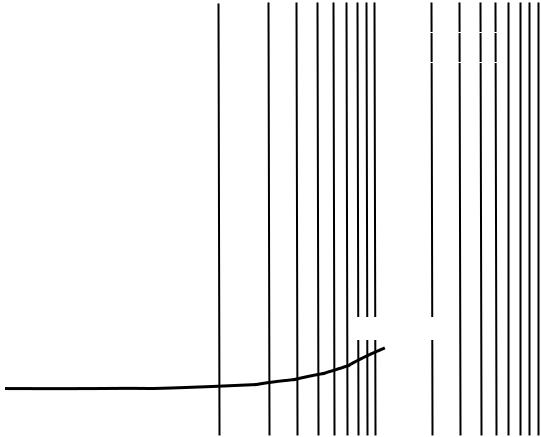
**EXTERNAL CLOCK**

The CLK input of the RS100 may be driven directly from

74 HC, 4000B series buffers (such as 4049) or from LS TTL with a 5.6 kΩ pull-up resistor. When conversion is complete, the internal clock is disabled even if the external clock is still ap-plied. This means that the external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

The RS100 is specified for operation at a 5 µs conversion rate; with a 4 MHz input clock frequency. If the part is operated at slower clock frequencies, it may result in slightly degraded accu-racy performance from the part. This is a result of leakage ef-fects on the hold capacitor. Figure 14 shows a typical plot of accuracy versus conversion time for the RS100.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **2.5** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **TA = +25**8**C** |  |  |  |
| **–LSB** | **2.0** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **ACCURACY** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **1.5** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **RELATIVE** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **1.0** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **RS100KN** | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **0.5** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **0** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | **10** | | |  | **50** | | |  |  | **100** | | **500** | **1000** | | **5000 10000** | | |  |
|  | **5** | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | **CONVERSION TIME –**m**s** | | | | | | | | | |  |  |  |  |



*Figure 14. Accuracy vs. Conversion Time*

**RS100**

**UNIPOLAR OPERATION**

The basic operation for the RS100 is in the unipolar single supply mode. Figure 15 shows the circuit connections to achieve this, while the nominal transfer characteristic for unipolar opera-tion is given in Figure 16. Since the offset and full-scale errors on the RS100 are very small, in many cases it will not be nec-essary to adjust out these errors. If calibration is required, the procedure is as follows:

**Offset Adjust**

Offset error adjustment in single-supply systems is easily achiev-able by means of the offset null facility of an op amp when used as a voltage follower for the analog input signal, AIN. The op amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0 V (e.g., TLC271). To adjust for zero offset, the input signal source is set to +4.8 mV (i.e., 1/2 LSB) while the op amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

**Full-Scale Adjust**

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445 V (i.e., Full-Scale Voltage –3/2 LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111. . . 11.

**BIPOLAR OPERATION**

The circuit of Figure 17 shows how the RS100 can be config-ured for bipolar operation. The output code provided by the RS100 is offset binary. The analog input voltage range is

* 5 V, although the voltage appearing at the AIN pin of the RS100 is in the range 0 V to +2.46 V. Figure 18 shows the transfer function for bipolar operation. The LSB size is now

39.06 mV. Calibration of the bipolar operation is outlined be-low. Once again, because the errors are small, it may not be necessary to adjust them. To maintain specified performance without the calibration, all resistors should be 0.1% tolerance with R4 and R5 replaced by one 3.3 kΩ resistor and R2 and R3 replaced by one 2.5 kΩ resistor.

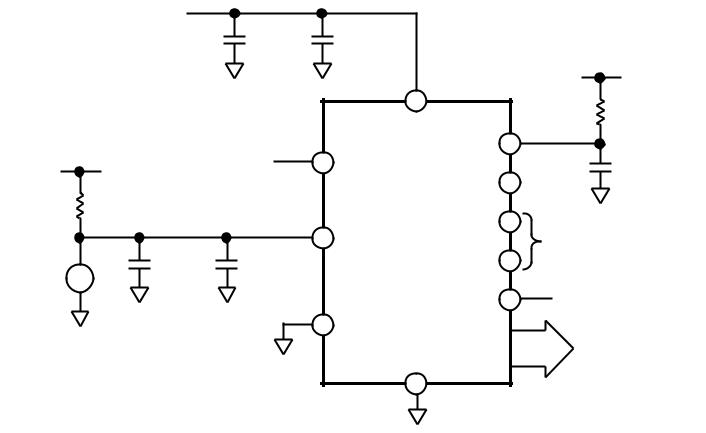
**Offset Adjust**

Offset error adjustment is achieved by applying an analog input voltage of –4.9805 V (–FS +1/2 LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

**Full-Scale Adjust**

Full-scale or gain adjustment is made by applying an analog input voltage of +4.9414 V (+FS –3/2 LSB). Resistor R4 is then adjusted until the output code flickers between 111 . . . 10 and 111. . . 11.

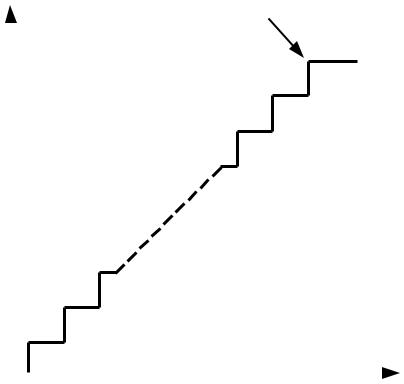
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **+5V** |  |  |  |  |
|  |  | **47**m**F** | **0.1**m**F** | **+5V** |  |
|  |  | **A** | **A** |  |
|  |  | **RCLK** |  |
|  |  |  |  |  |
|  |  |  | **VDD** | **100k**V**, 1%** |  |
| **+5V** |  | **+2.46V** | **CLK** | **CCLK** |  |
|  | **AIN** |  |
|  |  | **MAX** | **BUSY** | **100pF, 2%** |  |
| **3.3k**V |  | **+1.23V** | **RS100 CS** | **D** |  |
|  |  | **CONTROL** |  |
| **+** |  |  | **VREF** |  |
| **47**m**F** | **0.1**m**F** | **RD** | **INPUTS** |  |
| **AD589** |  |  |
|  |  |  | **+5V** |  |
| **–** | **A** | **A** | **TP** |  |
| **A** |  |  | **AGND** | **DB7–DB0** |  |
|  |  | **A** | **DGND** |  |
|  |  | **DATA OUT** |  |



**D**

*Figure 15. Unipolar Configuration*

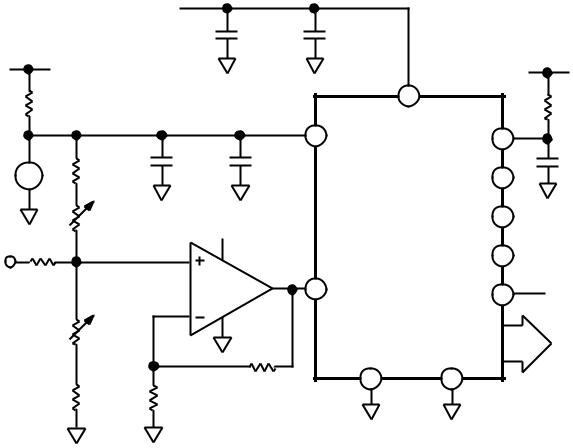
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **OUTPUT** | | | | | | | | | | | |  |  |  |  |  | **FULL SCALE** | | | | | | | | | | | | |  |  |  |  |  |  |
| **CODE** | | | | | | | | | | | |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | **TRANSITION** | | | | | | | | | | | | |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **11111111** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **11111110** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **11111101** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **FS = 2VREF** | | | | | | | | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **00000011** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **1LSB =** | | | | | | | **FS** | | | | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **256** | |  |  |  |  |
| **00000010** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **00000001** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **00000000** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | **1LSB** | | | **3LSBs** | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **FS** | | |  |
|  |  |  |  |  |  | **2LSBs** | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **FS –1LSB** | | | | | | | |  |



**AIN, INPUT VOLTAGE (IN TERMS OF LSBs)**

*Figure 16. Nominal Transfer Characteristic for Unipolar Operation*

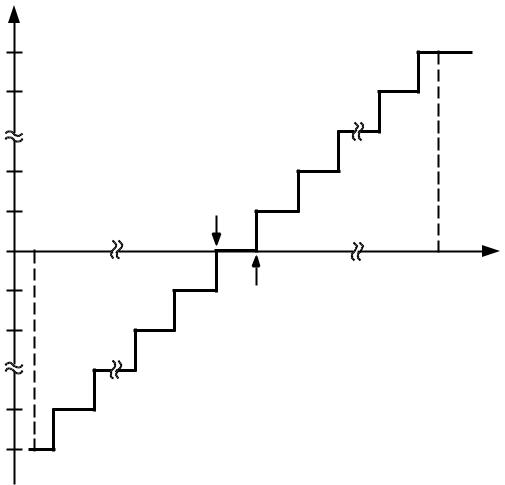
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  | **+5V** | **+** |  |  |  |  |  |  |
|  |  |  |  | **47**m**F** | | **0.1**m**F** |  |  |  |
|  | **+5V** |  |  |  |  | **+5V** |  |
|  |  |  |  | **A** |  | **A** |  |  |
|  |  |  |  |  |  |  | **RCLK** |  |
|  | **R8** |  |  |  |  |  |  |  |  |
|  | **3.3k**V | |  |  |  |  | **VDD** |  | **100k**V**, 1%** |  |
|  | **+** | **R2** | **47**m**F** | | **0.1**m**F** | | **VREF** | **CLK** | **CCLK** |  |
| **AD589** |  | **BUSY** | | **100pF, 2%** |  |
| **–** | **2.2k**V |  |  |  |  |  |
|  |  | **A** |  |  | **A** | **RS100** | **CS** | **D** |  |
|  | **A** | **R3** |  | **+5V** | |  |  |  |
| **INPUT** |  | **500**V |  |  |  |  |  | **RD** |  |  |
|  |  |  |  |  |  |  |  |  |
| **VOLTAGE** |  |  |  |  |  |  |  |  |  |
| **R1** |  |  | **TLC271** | | | **AIN** |  | **+5V** |  |
|  |  |  | **TP** |  |
|  | **10k**V |  |  |  |
|  |  |  |  |  |  |  |
|  |  | **R4** |  |  | **A** |  | **AGNDDGND** | | **DB7–DB0** |  |
|  |  |  |  |  | **DATA OUT** |  |
|  |  | **500**V |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  | **R5** | **R6** |  |  | **R7** |  |  |  |  |
|  |  | **3k**V | **2.5k**V | | **2.5k**V | | **A** | **D** |  |  |
|  |  |  |  |  |  |  |  |  |
|  |  | **A** | **A** |  |  |  |  |  |  |  |



*Figure 17. Bipolar Configuration*

**OUTPUT**

**CODE**



**111...111**

**111...110**

|  |  |  |  |
| --- | --- | --- | --- |
| **100...010** |  |  |  |
| **100...001** | **–1/2LSB** |  |  |
|  |  |  |
| **100...000** | **–FS** | **AIN** |  |
|  |  |
|  | **+FS –1LSB** | |  |
| **011...111** | **+1/2LSB** |  |  |
|  |  |  |
| **011...110** | **FS = 5V** | **FS** |  |
|  | **1LSB =** |  |
|  |  | **256** |  |
| **000...001** |  |  |  |
| **000...000** |  |  |  |

*Figure 18. Nominal Transfer Characteristic for Bipolar Operation*

**RS100**

**APPLICATION HINTS**

1. NOISE: Both the input signal lead to AIN and the signal return lead from AGND should be kept as short as possible to minimize input-noise coupling. In applications where this is not possible, either a shielded cable or a twisted pair transmis-sion line between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. In general, the source resistance should be kept below 2 kΩ. Larger values of source resistance can cause undesired system noise pickup.
2. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. Both the analog input and the reference input should be screened by AGND. A single point analog ground separate from the logic system ground, should be established at or near the RS100. This single point analog ground subsystem should be con-nected to the digital system ground by a single-track connec-tion only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

**RS100 WITH AD589 REFERENCE**

The RS100 8-bit A/D converter features a total unadjusted error specification over its entire operating temperature range. This total unadjusted error includes all errors in the A/D con-verter—offset, full scale and linearity. The one feature not pro-vided on the RS100 is a voltage reference. This section discusses the use of the AD589 bandgap reference with the RS100, and gives the combined reference and ADC error budget over the full operating temperature range. This allows the user to compare the combined AD589/RS100 errors to ADCs whose specifications include on-chip references.

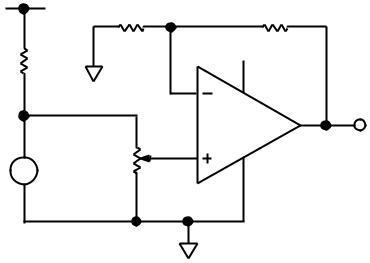
Two distinct application areas exist. The first is where the refer-ence voltage and the analog input voltage are derived from the same source. In other words, if the reference voltage varies, the analog input voltage range varies by a ratioed amount. In this case, the user is not worried about the absolute value of the reference voltage. The second case is where changes in the refer-ence voltage are not matched by changes in the analog input voltage range. Here, the absolute value of the reference voltage, and its drift over temperature, are of prime importance. Both applications are discussed below.

If the analog input range varies with the reference voltage, the part is said to be operating ratiometrically. This is representative of many applications. If the reference is on-chip, and the user does not have access to it, it is not possible to get ratiometric operation. Since the RS100 uses an external reference, it can be used in ratiometric applications. However, because the part is specified with a reference of +1.23 V ± 5%, then the voltage range for ratiometric operation is limited.

The error analysis over temperature of ratiometric applications is different from nonratiometric ones. Since the reference and analog input voltage range are ratioed to each other, tempera-ture variations in the reference are matched by variations in the analog input range. Therefore, the AD589 contributes no addi-tional errors over temperature to the system errors, and the combined total unadjusted error specification for the AD589 and RS100 is as per the total unadjusted error specification in this data sheet.

With nonratiometric applications, however, the analog input range stays the same if the reference varies and a full-scale error is introduced. The amount by which the reference varies deter-mines the amount of error introduced. The AD589 is graded on temperature coefficient; therefore, selection of different grades allows the user to tailor the amount of error introduced to suit the system requirements. The reference voltage from the AD589 can lie between 1.2 V and 1.25 V. This reference voltage can be adjusted for the desired full-scale voltage range using the circuit outlined in Figure 19. For example, if an analog input voltage range of 0 V to +2.46 V is required, the reference should be adjusted to +1.23 V. Once the reference is adjusted to the de-sired value at 25°C, the total error is as per the total unadjusted error specification on the RS100 specification pages. (To reduce this still further, offset and full-scale errors of the RS100 can be adjusted out using the calibration procedure outlined in this data sheet.)

**+5V**



**10k**V**\*** **1k**V**\***

**+5V**

**6.8k**V

**TLC271\***

**+**

**10k**V**\***

**AD589**

**–**

**\*ONLY REQUIRED IF IT IS NECESSARY TO ADJUST THE ABSOLUTE VALUE OF REFERENCE VOLTAGE.**

*Figure 19. Reference Adjust Circuit*

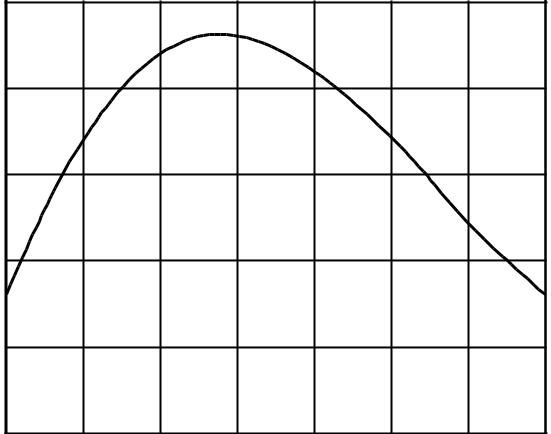
However, it is as the temperature varies from 25°C that the AD589 starts to introduce errors. The typical temperature char-acteristics of the AD589 are shown in Figure 20. The tempera-ture coefficients (TCs) represent the slopes of the diagonals of

the error band from +25°C to TMIN and +25°C to TMAX. The AD589 TC is specified in ppm/°C max and is offered in four

different grades.

**RS100**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **1.2370** |  |  |  |  |  |  |  |  |
|  | **1.2365** |  |  |  |  |  |  |  |  |
| **– V** |  |  |  |  |  |  |  |  |  |
| **VOLTAGE** | **1.2360** |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| **OUTPUT** | **1.2355** |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | **1.2350** |  |  |  |  |  |  |  |  |
|  | **1.2345** | **–25** | **0** | **25** | **50** | **75** | **100** | **125** |  |
|  | **–50** |  |



**TEMPERATURE –**8**C**

*Figure 20. Typical AD589 Temperature Characteristics*

The effect the TC has on the system error is that it introduces a full-scale error in the ADC. This, in turn, affects the total unad-justed error specification. For example, using the AD589KH with a 50 ppm/°C max TC the change in reference voltage from 25°C to 70°C will be from 1.23 V to 1.22724 V, a change of –

2.76 mV. This results in a change in the full-scale range of the ADC of –5.52 mV, since the full-scale range on the RS100 is

2 VREF. Because the LSB size for the RS100 is 9.61 mV, the AD589 introduces an additional full-scale error of –0.57 LSBs

on top of the existing full-scale error specification for the ADC. Since the total unadjusted error specification for the ADC includes the full-scale error, there is also a corresponding in-crease in the total unadjusted error of –0.57 LSBs. The change in reference voltage at 0°C is –1.5 mV, resulting in a full-scale change of –3 mV or –0.31 LSBs worth of full-scale error. Table I shows the amount of additional total unadjusted error, which is introduced by the temperature variation of the AD589, for different grades and for different temperature ranges. This table applies only to nonratiometric applications, because the tem-perature variation of the reference does not affect the system error in ratiometric applications as outlined earlier. It shows the amount of error introduced over TMIN to TMAX for a system in which the reference has been adjusted to the desired value at

25°C. The final or right-most column of the table gives the total combined error for the AD589 and the top grade RS100.

Taking the 25°C measurement as the starting point, the full-scale error introduced is always in the negative direction whether the temperature goes to TMIN or TMAX. This can be seen from the AD589 temperature characteristic shown in Fig-ure 20. If the reference voltage is adjusted for 1.23 V at 45°C (for the 0°C to +70°C range) and 75°C (for the –55°C to

+125°C range) the magnitude of the error introduced is reduced since it is distributed in both the positive and negative direc-tions. Alternatively, this can be achieved not by adjusting at these temperatures, which would be impractical, but by adjust-ing the reference to 1.231 V instead of 1.23 V (for the extended temperature range) at 25°C. This has the required effect of distributing the plot of Figure 20 more evenly about the desired value.

An additional error source is the mismatch between the tem-perature coefficients (TCs) of the 10 kΩ and 1 kΩ resistors in the feedback loop of the TLC271. If these resistors have

* 50 ppm/°C absolute TCs, the worst case difference in drift be-tween both resistors is 100 ppm/°C. From +25°C to +125°C, this introduces a worst case shift of 1.22 mV, which results in an addi-

tional full-scale error of 0.25 LSB. If ± 25 ppm/°C resistors are used, then the worst case error is 0.13 LSB. Over the 0°C to

+70°C range, the ± 50 ppm/°C resistors introduce an additional full-scale error of 0.11 LSB. All these errors are worst case and assume that the resistance values drift in opposite directions. In practice, resistors of the same type, and from the same manufac-turer, would drift in the same direction and hence the above error would be considerably reduced. An additional error source is the offset drift of the TLC271. This is significant only over the –55°C to +125°C range and, even in this case, it contrib-utes <0.1 LSB worth of full-scale error.

The error outlined in the right-hand column of Table I is a total unadjusted error specification, excluding resistor and offset drift (the effect of these can be controlled by the user). It consists of errors from two error sources: a ±l LSB contribution from the RS100 (including full-scale, offset and relative accuracy er-rors), and the remainder is a full-scale error introduced by the AD589. It is important to note that the variation of the AD589 voltage only introduces a full-scale error; the relative accuracy (or endpoint nonlinearity) of the system, with a top grade RS100, is still ±1/2 LSB (i.e., 8-bits accurate).

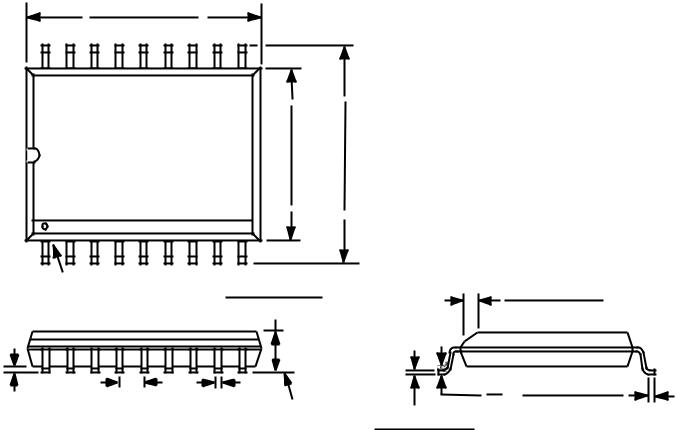
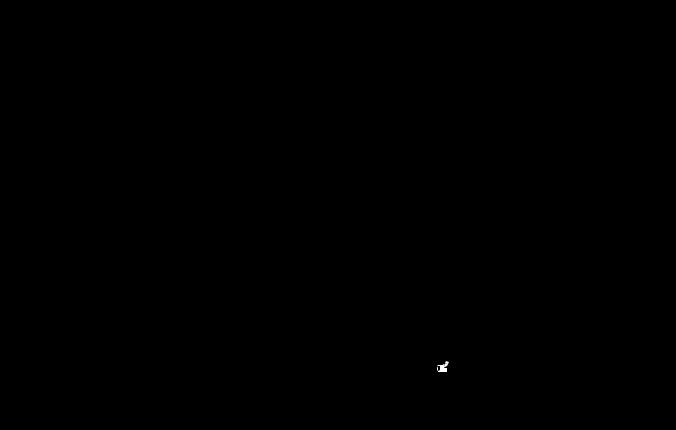
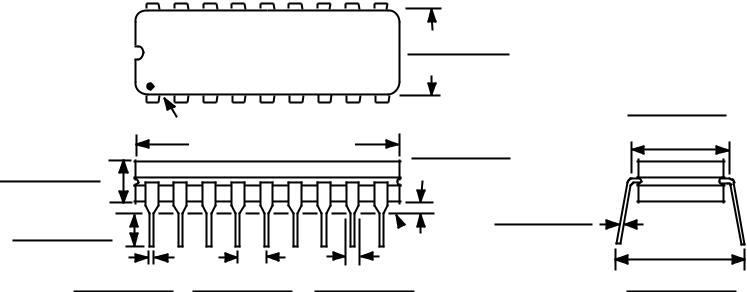
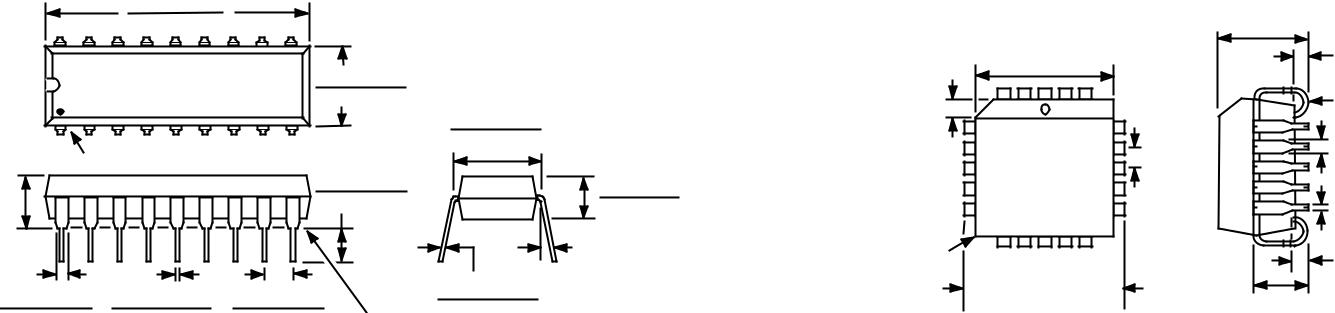
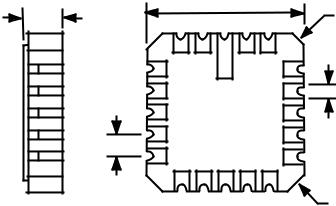
**Table I. AD589/RS100 Error over Temperature (Nonratiometric Applications)**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | **Full-Scale Error Introduced** | **Combined Worst Case** |
| **AD589** | **Temperature** | **by AD589 @ TMAX** | **AD589/RS100** |
| **Grade** | **Range** | **(Worst Case)** | **T.U.E. @ TMAX** |
| AD589JH | 0°C to +70°C | –1.15 LSB | –2.15 LSB |
| AD589KH | 0°C to +70°C | –0.57 LSB | –1.57 LSB |
| AD589LH | 0°C to +70°C | –0.29 LSB | –1.29 LSB |
| AD589MH | 0°C to +70°C | –0.115 LSB | –1.115 LSB |
| AD589SH | –55°C to +125°C | –2.56 LSB | –3.56 LSB |
| AD589TH | –55°C to +125°C | –1.28 LSB | –2.28 LSB |
| AD589UH | –55°C to +125°C | –0.64 LSB | –1.64 LSB |
|  |  |  |  |

\*Excluding resistor and offset drift.

**RS100**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  | **OUTLINE DIMENSIONS** | | | | | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | Dimensions shown in inches and (mm). | | | | | | |  |  |  |  |  |  |  |
|  |  | **18-Lead Plastic DIP** | | | | |  |  |  |  |  |  |  |  | **20-Lead PLCC** | | | | |  |
|  |  |  |  | **(N-18)** | |  |  |  |  |  |  |  |  |  |  | **(P-20A)** | | |  |  |
|  | **0.91 (23.12)** | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **0.173** 6**0.008** | |  |
|  | **0.89 (22.61)** | |  |  |  |  |  |  |  |  |  |  |  | **0.353** 6**0.003** | | |  | **(4.388** 6**0.185)** | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | **0.020** |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **18** |  |  |  | **10** |  |  |  |  |  |  |  |  |  | **(8.966** 6**0.076) SQ** | | | |  | **(0.51) MIN** |  |
|  |  |  |  | **0.26 (6.61)** | |  |  |  |  |  |  |  |  |  |  |  |  |  | **0.035** 6**0.01** |  |
|  |  |  |  | **9 0.24 (6.10)** | |  |  |  |  |  |  |  | **0.045** 6**0.003** |  |  |  |  |  |  |
| **1** |  |  |  | **0.306 (7.78)** | |  |  |  |  |  |  | **3** | **19** |  |  | **R (0.89** 6**0.25)** |  |
|  |  |  |  |  |  | **0.294 (7.47)** | |  |  |  |  |  | **(1.143** 6**0.076)** | **4** | **PIN 1** | **18** | |  |  |  |
| **PIN 1** | |  |  |  |  |  |  |  |  |  |  |  | **IDENTIFIER** | |  | **0.050** | **0.029** 6**0.003** |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | **TOP VIEW** | |  | **(1.27)** | **(0.737** 6**0.076)** |  |
| **0.18** |  |  |  | **0.175 (4.45)** | |  |  | **0.14 (3.56)** |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  | **(PINS DOWN)** | |  |  | **0.017** 6**0.004** |  |
| **(4.58)** |  |  |  | **0.12 (3.05)** | |  |  | **0.12 (3.05)** |  |  |  |  |  | **8** |  | **14** | |  |  |
| **MAX** |  |  |  |  |  |  |  |  |  |  |  |  | **9** |  | **(0.432** 6**0.101)** |  |
|  |  |  |  |  |  |  | **15**8 |  |  |  |  | **0.020** | | **13** |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **0.025 MIN** |  |
|  |  |  |  |  |  |  |  | **0** |  |  |  |  | **(0.51)** | |  |  |  |  |  |
|  |  |  |  |  |  | **0.12 (0.305)** | |  |  |  |  |  | **MAX0.390** 6**0.005** | | | |  |  | **(0.64)** |  |
| **0.065 (1.66)** | **0.02 (0.508)** | | **0.105 (2.67)** | |  |  |  |  |  |  |  | **(9.905** 6**0.125) SQ** | | | |  | **0.105** 6**0.015** |  |
| **0.045 (1.15)** | **0.015 (0.381)** | | **0.095 (2.42)** | | **SEATING** | **0.008 (0.203)** | |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | **(2.665** 6**0.375)** |  |
|  |  |  |  |  | **PLANE** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | **18-Lead Cerdip** | | |  |  |  |  |  |  |  |  |  | **20-Terminal LCCC** | | | | |  |
|  |  |  |  | **(Q-18)** | |  |  |  |  |  |  |  |  |  |  | **(E-20A)** | | |  |  |
|  | **18** |  |  |  | **10** |  |  |  |  |  |  |  | **0.082** 6 **0.018** | | | **0.350** 6 **0.008** | | |  |  |
|  |  |  |  |  |  |  |  |  |  |  | **(2.085** 6 **0.455)** | | | **(8.89** 6 **0.20) SQ** | | | **0.020** 3 **45**8 |  |
|  |  |  |  |  | **0.310 (7.874)** | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **(0.51** 3 **45**8**)** |  |
|  |  |  |  |  | **0.260 (6.604)** | |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **1** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **REF** |  |
|  |  |  |  | **9** |  |  |  |  |  |  |  |  |  |  | **19** |  | **3** |  |
|  |  |  |  |  |  | **0.320 (8.128)** | |  |  |  |  |  |  | **20** |  |  |
|  | **PIN 1** | |  |  |  |  |  |  |  |  |  |  |  | **18** | **4** | **0.025** 6 **0.003** |  |
|  |  |  |  |  |  | **0.290 (7.366)** | |  |  |  |  |  |  |  |  | **1** |  |
|  |  | **0.950 (24.13) MAX** | | | **0.060 (1.524)** | |  |  |  |  |  |  |  |  |  | **(0.635** 6 **0.075)** |  |
|  |  |  |  |  |  |  |  |  |  |  |  | **BOTTOM** | |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **0.180 (4.572)** |  |  |  |  | **0.015 (0.381)** | |  |  |  |  |  |  |  |  |  |  | **VIEW** | |  |  |
| **0.140 (3.556)** |  |  |  |  |  | **0.015 (0.381)** | |  |  |  |  |  |  |  |  | **14** |  | **8** |  |  |
| **0.200 (5.080)** |  |  |  |  |  |  |  |  |  |  |  |  | **0.050** | **13** |  | **9** | **0.040** 3 **45**8 |  |
|  |  |  |  |  | **0.008 (0.203)** | |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **(1.02** 3 **45**8**)** |  |
| **0.125 (3.175)** |  |  |  |  |  |  |  |  |  |  |  |  | **(1.27)** |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **REF 3 PLCS** |  |
| **0.023 (0.584)** | | **0.110 (2.794)** | | **0.070 (1.778)** | |  |  | **0.400 (10.160)** | |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| **0.015 (0.381)** | | **0.090 (2.286)** | | **0.030 (0.762) SEATING** | | |  | **0.330 (8.382)** | |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | **PLANE** | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | **18-Lead SOIC** | | | | | |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | **(R-18)** | | | |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | **0.4625 (11.75)** | | |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | **0.4469 (11.35)** | | |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | **18** |  | **10** |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | **1** |  | **9** | **29920. (7.60)** | **0. (7.40)2914** | **0. (10.65)4193** | **39370. (10.00)** |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | **PIN 1** |  | **0.1043 (2.65)** | | | |  | **0.0291 (0.74)** | | |  |  |  |  |  |
|  |  |  |  |  |  |  |  | **0.0926 (2.35)** | | | |  | **0.0098 (0.25)**3 **45**8 | | | |  |  |  |  |
|  |  |  |  |  | **0.0118 (0.30)** | | **0.0500 0.0192 (0.49)** | | |  |  |  | **8**8 | **0.0500 (1.27)** | |  |  |  |  |  |
|  |  |  |  |  | **SEATING** | | | **0.0125 (0.32) 0**8 | **0.0157 (0.40)** | |  |  |  |  |  |
|  |  |  |  |  | **0.0040 (0.10)** | | **(1.27)** | **0.0138 (0.35)** | | **PLANE** | |  | **0.0091 (0.23)** |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  | **BSC** |  |  |  |  |  |  |  |  |  |  |  |  |



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